THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 19

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Ex parte MITSUHARU OHKI

Appeal No. 97-1182
Application No. 08/150,371[1]

ON BRIEF

Before THOMAS, KRASS, and SMITH, Administrative Patent Judges.

KRASS, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal from the final rejection of claims 1 through 22, all of the claims in the application.

[1] Application for patent filed November 10, 1993.

The invention is directed to a method and apparatus for multiplying matrix data.

Representative independent claim 1, the independent method claim, is reproduced as follows:

1. A method of multiplying matrix data comprising the steps of:

(a) inputting an input vector data signal to a matrix multiplying circuit,

(b) multiplying said input vector data signal by a first constant matrix with said matrix multiplying circuit, and

(c) outputting from said matrix multiplying circuit the result of the multiplying step (b) as an output vector signal,

wherein said multiplying by a constant matrix step (b) includes:

(b) (1) resolving with said matrix multiplying circuit said first constant matrix into a first group of constant matrices;

(b) (2) further resolving with said matrix multiplying circuit one matrix of said first group of constant matrices into at least three finally-resolved constant matrices, each finally-resolved constant matrix being composed of elements selected from the following group 0, +1, and - 1; and

(b) (3) multiplying said input vector signal with said one matrix, said one matrix being resolved to each

finally-resolved constant matrix, in stages by performing adding and subtracting steps with an adding/subtracting circuit.

The examiner relies on the following reference:

Watari 4,839,844 Jun. 13, 1989

Claims 1 through 22 stand rejected under 35 U.S.C. 112, second paragraph, as being indefinite. Claims 1, 2, 5 through 7, 10 and 17 through 22 stand further rejected under 35 U.S.C. 102(b) as anticipated by Watari. Additionally, claims 1 through 5, 11, 13, 14, 17, 19 and 20, all of the method claims, stand rejected under 35 U.S.C. 101 as being directed to nonstatutory subject matter.

Reference is made to the brief and answer for the respective positions of appellant and the examiner.

OPINION

Turning first to the rejection of claims 1 through 22 under the second paragraph of 35 U.S.C. 112, the examiner holds these claims to be indefinite. The answer contains only the following reasoning with regard to this rejection:

Each of the independent claims is misdescriptive because they call for the matrix multiplying circuit to resolve the constant matrix into a plurality of matrices. While the matrix multiplying circuit multiplies the input vector by the resolved matrices, the multiplying circuit does not perform the resolving. In fact, there is no disclosure of a means to perform the resolving [answer - page 5].

We disagree with the examiner's reasoning. The examiner apparently is of the opinion that the "multiplying circuit" is only a circuit for multiplying and cannot serve any other purpose. However, as reference to the disclosure and further study of the claim language reveal, the claimed "matrix multiplying circuit" is merely the box into which the input vector data signal is input and from which the final output of the entire operation is taken. In other words, the claimed "matrix multiplying circuit" is the element that performs all of the multiplying and resolving operations. See claim 1, for example, where the basic method comprises inputting the input vector data signal into a "box," if you will, which performs the multiplication by a first constant matrix, and outputting from the "box," or matrix multiplying circuit, an output

vector signal. The remainder of the claim sets forth what is included in the "box." That is, the step of multiplying the input vector data signal by a first constant matrix with the matrix multiplying circuit is not merely a simple multiplication, but, as set forth in claim 1, rather a process which includes resolving, further resolving, and multiplying... Accordingly, it is clear that the matrix multiplying circuit is more than a mere multiplier. It includes the claimed resolving functions also. Thus, contrary to the examiner's position, the matrix multiplying circuit *does* perform the claimed resolving.

We now turn to the rejection of the method claims under 35 U.S.C. 101 as being directed to nonstatutory subject matter.

We will not sustain the rejection of claims 3, 4, 11, 13, 14, 19 and 20 under 35 U.S.C. 101 but we will sustain the rejection of claims 1, 2, 5 and 17 under 35 U.S.C. 101.

With regard to claims 3, 4, 11, 13, 14, 19 and 20, these claims recite that the input vector signal comprises an "image" signal. The image signal is transformed from real space to frequency space. Because it is an "image" signal

that is being operated upon, it is clear that the claimed subject matter is directed to a practical application of the algorithm which operates on the image signal. The algorithm produces a "useful, concrete and tangible result" - the transformation of an image signal. Accordingly, the subject matter recited in claims 3, 4, 11, 13, 14, 19 and 20 is statutory, within the meaning of 35 U.S.C. 101. See State Street Bank & Trust Co., v. Signature Financial Group, Inc., 149 F.3d 1368, 1373, 47 USPQ 2d, 1596, 1601 (Fed. Cir. 1998). However, when we analyze claims 1, 2, 5 and 17 under 35 U.S.C. 101, we reach a different result.

Claim 1 does not recite any image signal but, rather, only an "input vector data signal." One could argue that reference to the disclosure would indicate that this signal is intended to be an "image" signal. However, reference to the instant claims appears to tell a different story. Clearly, since dependent claim 3 adds the further limitation that the "input vector signal comprises an image signal," appellant intends the recitation of a mere "input vector data signal" in independent claim 1 to have a much broader meaning. That

broader interpretation does not appear to dictate that the "input vector signal" be a physical signal of any sort.

Thus, while appellant may argue [brief - page 16] that claim 1 is directed to a method in which a signal is transformed from one state to a second state, more specifically, that an input vector signal is transformed into an output vector signal, citing Arrythmia Research Technology, Inc. v. Corazonix Corporation, 958 F.2d 1053, 1059, 22 USPQ2d 1033, 1038 (Fed. Cir. 1992) as authority for the statutory nature of such a claim, we disagree. The signal in Arrythmia was, indeed, representative of a physical signal - signals related to the functioning of a human heart. By contrast, the general recitation of an "input vector data signal" in instant claim 1 is not tied, by any claim language, to any specific physical phenomena or to any practical application of such a signal.

Claim 1 merely calls for inputting a signal, albeit a "vector data signal" into a matrix multiplying circuit which then mathematically manipulates that signal to result in a mathematical matrix. There is no indication in the claim of any connection to a physical thing or a practical application

of the mathematical manipulation of one matrix to result in another matrix.

Appellant argues [brief - page 17] that the claimed process is the process by which a circuit operates, such as the claimed matrix multiplying circuit, and, therefore, the process must also be directed to statutory subject matter. However, the circuitry, or apparatus, claims, were not rejected by the examiner (and, accordingly, are not before us on 35 U.S.C. 101 grounds), the examiner apparently concluding that such claims, being directed to physical structure, are not subject to a rejection based on 35 U.S.C. 101 on nonstatutory grounds. Claims 1, 2, 5 and 17 are not directed to any such structure or to any practical application of the claimed algorithm.

One might argue that the term "vector data signal" implies some practical application because a "signal" must evolve from some physical manifestation or that a "vector" is indicative, somehow, of a physical signal. However, in our view, as broadly claimed, a "signal" could be nothing more than input data and a "vector" implies nothing more than a mathematical value having some magnitude and direction. Had

appellant desired to have the claim construed to include some practical application of the recited algorithm or a physical structure, appellant could easily have presented or amended the claims to do so. We find nothing within claims 1, 2, 5 and 17 which would take the claims out of the mathematical algorithm exception to statutory classes of invention recited in 35 U.S.C. 101.

Appellant does recite, at the end of claim 1, that the recited "adding and subtracting" steps are carried out "with an adding/subtracting circuit." While one might argue that the recitation of such "structure" would make the subject matter as a whole statutory, within the meaning of 35 U.S.C. 101, we do not so hold. In our view, such a limitation amounts to no more than a gratuitous recitation of a general circuit for the purpose of circumventing the rejection under 35 U.S.C. 101 and amounts to no more than an attempt to exalt form over substance. The mere recitation of "an adding/subtracting circuit" adds nothing to the claimed subject matter because the claimed method already recites "performing adding and subtracting steps." Thus, anything that would perform this function may be characterized,

generally, as "an adding/subtracting circuit." Accordingly, the granting of a patent on such a claim would act to preempt the use of any and all means to perform the already-held nonstatutory method of claim 1 since any means to perform the adding and subtracting steps would constitute "an adding/subtracting circuit."

Since one of the public policies behind the mathematical algorithm exception to 35 U.S.C. 101 is not to preempt others from employing mathematical algorithms which are scientific tools which should be available to anyone and instant claim 1 has been held to be drawn to such a nonstatutory mathematical algorithm, unrelated to any practical application of said algorithm, it would appear illogical to impart statutory status to otherwise nonstatutory subject matter by the mere inclusion of "an adding/subtracting circuit" where such language, if granted patented status, would amount to a preemption of the mathematical algorithm of claim 1 from being performed by any and all means for adding and subtracting. Of course, the situation might be different if the "adding/subtracting circuit" was recited as comprising some specific structure for adding and subtracting.

Turning, finally, to the rejection under 35 U.S.C. 102(b), we will not sustain this rejection.

In order for a proper rejection to rest under this statutory section, the reference must teach or suggest each and every claim limitation. While Watari does appear to be fairly pertinent to the claimed subject matter, in generally disclosing the multiplication of a vector data signal by a constant matrix and the outputting of a result, the instant claims call for much more.

The instant claims require the resolving of the first constant matrix into a first group of constant matrices and then a further resolving of one of the matrices of the first group of constant matrices into at least three finally-resolved constant matrices. Contrary to the examiner's position, we find no such resolving and further resolving in Watari.

From column 4 of Watari, it is apparent that Watari does a first resolving of a constant matrix C into a first group of constant matrices, G1....Gn. However, there is no further resolving of any one of these matrices G1...Gn into at least three finally-resolved constant matrices. The examiner's

interpretation that a group G1, G2 and G3, together, form a first group of matrices which then may be further resolved into separate G1, G2 and G3 constant matrices is, in our view, unreasonable since the lumping of three of the constant matrices together and then separating them does not constitute a "further resolving," as claimed.

We also note, that with regard to some of the dependent claims where the examiner admits that the reference does not disclose "image" data but that "transforming is the same whether the signal represents image or audio data," and that the reference does not disclose DCT or IDCT but that "transforming is the same whether it is Walsh, DCT, or IDCT," such reasoning by the examiner might have some place in a rejection under
35 U.S.C. 103, but such reasoning is not valid in a rejection based on anticipation under 35 U.S.C. 102(b).

Since Watari does not disclose or suggest each and every claimed limitation, we will not sustain the rejection under 35 U.S.C. 102(b).

CONCLUSION

We have not sustained the rejection under 35 U.S.C. 102(b) or the rejection under 35 U.S.C. 112, second paragraph. We also have not sustained the rejection of claims 3, 4, 11, 13, 14, 19 and 20 under 35 U.S.C. 101 but we have sustained the rejection of claims 1, 2, 5 and 17 under 35 U.S.C. 101.

Accordingly, the examiner's decision is affirmed-in-part.

No period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED-IN-PART

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| JAMES D. THOMAS<br>Administrative Patent Judge | ) |
| ERROL A. KRASS<br>Administrative Patent Judge | ) BOARD OF PATENT<br>) APPEALS<br>) AND<br>) INTERFERENCES |
| JERRY SMITH | ) |

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Appeal No. 97-1182

Application No. 08/150,371

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AFFIRMED-IN-PART

Prepared: September 21, 1999